

PAMS Technical Documentation

RAE-3 Series PDA

4. User Interfaces

AMENDMENT RECORD SHEET

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Abbreviations

AC	Alternating Current
BL8	RAE-3 Main PWB
BOC	Blue Oyster Cult
CMT	Cellular Mobile Transceiver
CCFL	Cold Cathode Fluorescent Lamp
DL2	Linda Display module including PWB and displays
ESD	Electro Static Discharge
FPC	Flexible Printed Circuit
FSTN	Film Compensated Super Twisted Nematic
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MCU	Micro Computer Unit
PWB	Printed Wiring Board
PDA	Personal Digital Assistant
UI	User Interface
UIF	User InterFace
UL2	DL2 PWB submodule

RAE-3 User Interface Structure

RAE-3 GSM900/GSM1800 Dual Band Communicator User Interface comprises the QWERTY keyboard module UL8 and the DL2 module with both displays.

User Interface DL2

This section describes the DL2 module. This module includes

- a PWB (UL2) with SMD components,
- PDA display (including CCFL backlight),
- CMT display with frame and lightguide and
- CMT keypad backlights.

DL2 is located in the cover side of RAE-3. Figures below describe the two sides of the module.

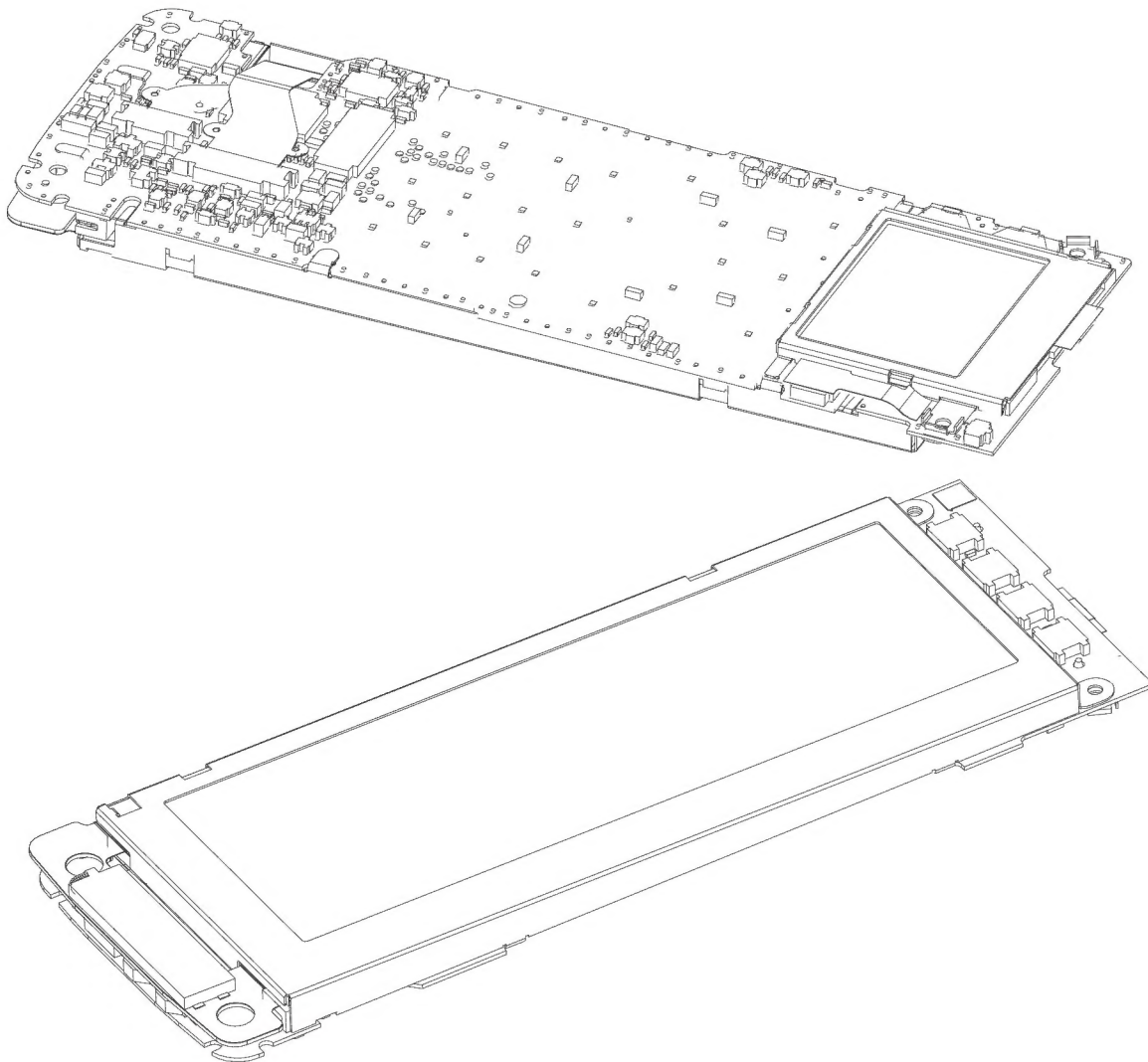


Figure 1. DL2 module

Main Components

DL2 main components include UL2 PWB with components, PDA display and CMT display.

Components on the module assembly include the following:

- Four layer, 0.6mm thick PWB (UL2) including:
 - PDA LCD CCFL backlight circuit.
 - Power circuit for PDA LCD bias voltages.
 - Power circuit and LEDs for CMT keypad and CMT display backlight.
 - Antenna clips and ground plane.
 - Coaxial cable connector for antenna cable.
 - 10-pin and 20-pin flex connectors for PDA display module.

- 50–pin flex connector for hinge flex.
- 10–pin flex connection for CMT display.
- 4–way stacker connection for piezo flex assembly.
- Pads for CMT keypad.
- PDA soft key switches.
- PDA LCD module including lightguide, piezo transformer FPC, CCFL and metal frame.
- CMT Display module including metal frame and lightguide.

DC Characteristics

Supply voltages and power consumption are listed below:

Pin / Conn.	Line Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
X1/1, X1/49, X1/50	VB	Battery Voltage	3.0	3.6	4.2	V	4.8V Absolute maximum
					210	mA	
X1/11	VBB	Logic voltage	2.7	2.8	2.9	V	
					20	mA	

Connections

The 50–way FPC connects the DL2 to the BL8 (system logic and RF board) via the hinge. It has all active signals for the DL2 module and supply pins. It is connected to the 50–pin board–to–board connector X1.

DL2 has coaxial cable connector for antenna cable. This co–axial cable goes through the hinge to the BL8 RF part.

X1 connector pinout

PIN/ Pins	Line Symbol	Parameter	Min.	Typ. / No m.	Max.	Unit	Active level	Function
1,49 50	VB	Battery voltage	3.0	3.6	4.2	V		Supply
11	VBB	Logic voltage	2.7	2.8	2.9	V		Supply
3, 7, 19, 26, 37, 38, 44, 48	GND	Ground		0		V		Supply
21	LCDPWR	PDA LCD Volt- ages switch	0 1.58V		0.88V VBB	V	Inactive Active	Input. High level turns on supply to display

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PIN/ Pins	Line Sym- bol	Parameter	Min.	Typ. / No m.	Max.	Unit	Active level	Function
16	GenSClk	Serial Clock for CMT display	0	3.25	4.0	MHz		Input
			0 0.7xVBB		0.3xVBB VBB	V	Low High	Input
18	GenSDIO	Serial Data for CMT display	0 0.7xVBB		0.3xVBB VBB	V	Low High	Input
46	Row5LCDC D	CMT display con- trol / data	0 0.7xVBB		0.3xVBB VBB	V	Control Data	Input. Low level se- lects com- mand regis- ter
15	LCDEN	CMT display en- able	0 0.7xVBB		0.3xVBB VBB	V	Active Inactive	Input. Low level en- ables writ- ing to the display
13	LCDRSTX	CMT display reset	0 0.7xVBB		0.3xVBB VBB	V	Active Inactive	Input. Low level resets the display
14	KBLIGHTS	CMT keypad and display backlight control	0 0.7xVBB		0.3xVBB VBB	V	Active Inactive	Input. High level turns lights on.
22	LCDDa0	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
2	LCDDa1	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
4	LCDDa2	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
33	LCDDa3	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
8	LCDDa4	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
31	LCDDa5	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
32	LCDDa6	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
6	LCDDa7	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
9	LCDDa8	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
5	LCDDa9	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
34	LCDDa10	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input

PIN/ Pins	Line Sym- bol	Parameter	Min.	Typ. / No m.	Max.	Unit	Active level	Function
20	LCDDa11	PDA display data	0 1.58V		0.88V VBB	V	Low High	Input
25	DISPClk	PDA display Pixel clock	8	8.66	10	MHz		
			0 1.58V		0.88V VBB	V	Low High	Input
35	LLCk	PDA display Line pulse	0	10.8	12.5	kHz		
			0 1.58V		0.88V VBB	V	Low High	Input
23	FSP	PDA display Frame pulse	0	51.5	59	Hz		
			0 1.58V		0.88V VBB	V	Low High	Input
10	LCDM	PDA display AC– modulation	0	10.8	15	kHz		
			0 1.58V		0.88V VBB	V	Low High	Input
24	DISPON	PDA display ON/ OFF	0 1.58V		0.88V VBB	V	Active Inactive	Input
36	LCD_TEM P	Connected to ground for color display detection.						Unused.
30	Col0	Keypad column 0	0 0.7xVBB		0.3xVBB VBB	V	Low High	Input
27	Col1	Keypad column 1	0 0.7xVBB		0.3xVBB VBB	V	Low High	Input
28	Col2	Keypad column 2	0 0.7xVBB		0.3xVBB VBB	V	Low High	Input
43	Col3	Keypad column 3	0 0.7xVBB		0.3xVBB VBB	V	Low High	Input
45	Col4	Keypad column 4	0 0.7xVBB		0.3xVBB VBB	V	Low High	Input
29	Row0	Keypad row 0	0 0.7xVBB		0.3xVBB VBB	V	Low High	Output
39	Row1	Keypad row 1	0 0.7xVBB		0.3xVBB VBB	V	Low High	Output
40	Row2	Keypad row 2	0 0.7xVBB		0.3xVBB VBB	V	Low High	Output
41	Row3	Keypad row 3	0 0.7xVBB		0.3xVBB VBB	V	Low High	Output

PIN/ Pins	Line Sym- bol	Parameter	Min.	Typ. / No m.	Max.	Unit	Active level	Function
42	Row4	Keypad row 4	0 0.7xVBB		0.3xVBB VBB	V	Low High	Output
17	LCDPWM	PDA LCD Con- trast control	0 0.7xVBB	50.7	0.3xVBB VBB	V KHz	Low High	Input
47	BACKPWM	PDA LCD Back- light control	0 0.7xVBB	335	0.3xVBB VBB	V Hz	Low High	Input

Antenna clip connector

DL2 has antenna clips that are connected to the antenna.

Pin	Line Symbol	Parame- ter	Minimum	Typical / Nominal	Maxi- mum	Unit	Notes
X1/1, X1/49, X1/50	VB	Battery Voltage	3.0	3.6	4.2	V	4.8V Ab- solute maximum

X2 connector pinout

Row driver features a 10-pin flex connector.

Pin	Line Sym- bol	Minimum	Typical / Nomi- nal	Maximum	Unit	Notes
1	GND		0		V	LCD driving level for Y driver IC
2	XINH	0 0.8 x VDDY	Logic 0 Logic 1	0.2 x VDDY VDDY	V	Line sub-sampling signal for Y driver IC
3	YSCL	0 0.9 x VDDY	Logic 0 Logic 1	0.1 x VDDY VDDY	V	Shift clock for Y driver IC
4	FRY	0 0.8 x VDDY	Logic 0 Logic 1	0.2 x VDDY VDDY	V	Output control for Y driver IC
5	VCCY	2.7	VCC-V5Y 3.3	4.5	V	High level supply voltage for Y driver IC
6	V5Y					Low level supply voltage for Y driver IC
7	NC					Not connected

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit	Notes
8	V0Y	8.0	V0Y–V5Y–VDD	33	V	LCD driving level for Y driver IC
9	VDD					LCD driving level for Y driver IC
10	DY	0 0.8 x VDDY	Logic 0 Logic 1	0.2 x VDDY VDDY		Shift start pulse for Y driver IC

X3 connector pinout

Column drivers feature a 20-pin flex connector.

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit	Notes
1	VCC				V	Logic supply for X driver
2	VDDH				V	LCD supply for X driver
3	D23	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
4	D22	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
5	D21	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
6	D20	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
7	GCP	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	PWM width control pulse for X driver
8	FR	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Output alternation signal for X drivers
9	LP	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Data load and shift pulse for X driver
10	RES	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	PWM counter reset signal for X driver
11	D03	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
12	D02	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
13	D01	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
14	D00	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal

Pin	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit	Notes
15	XSCL	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Shift clock for X driver
16	D13	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
17	D12	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
18	D11	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
19	D10	0 0.7 x VDDX	Logic 0 Logic 1	0.3 x VDDX VDDX	V	Digital video signal
20	GND		0		V	Logic Low signal for X driver, LCD low level for X driver

X6 connector pinout

X6 is a 4 way 'stacker' connector to piezo FPC.

Pin	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit	Function
1	Feedback	Feedback from CCFL output	0	0.84	1.54	V	Input
2	Piezo_in	Input to primary of piezo transformer	0	5	8	Vrms	Output
3	AGND			0		V	Supply
4	GND			0		V	Supply

X7 connector pinout

X7 is a 10 way flex connector to CMT LCD..

Pin	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes	Function
1	GND	Ground		0		V		Supply
2	VOOUT	DC/DC voltage converter output			9			Input
3	LCDRSTX	Reset	0		0.3xVBB		Active	Output
4,5	VBB	Supply voltage	2.7	2.8	2.9	V		Supply
					300	uA		
6	GenSClk	Serial clock input	203kHz	3.25MHz	3.25MHz	MHz		Output

Pin	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes	Function
6			0 0,7xVBB		0.3xVBB VBB	V	Low High	Output
7	GenSDIO	Serial data input	0 0.7xVBB		0.3xVBB VBB	V V	Low High	Output
8	Row5LCD CD	Control/display data flag input	0 0.7xVBB		0.3xVBB VBB		Control Data	Output
9	LCDEN	Chip select input	0 0.7xVBB		0.3xVBB VBB		Active Inactive	Output
10	OSC*	External clock for LCD					Connected to VBB on UL2	Inactive

RF connection

Pin	Line symbol	Parameter	Minimum frequency	Maximum frequency	Maximum power	Notes
	RF	Antenna feed cable	890 MHz	1880 MHz	33 dBm (peak) 28.8 dBm (average)	

Functional description

Power distribution and control signals

The following block diagram describes the distribution of power supplies within DL2.

Battery voltage VB is fed directly to the illumination LEDS (CMT keymat and CMT display)

The regulated band supply VBB generated on the BL8 module supplies the CMT display, control logic and PDA display supply.

A power switch is used to remove the voltage supply from the control logic and PDA display when the display is turned off.

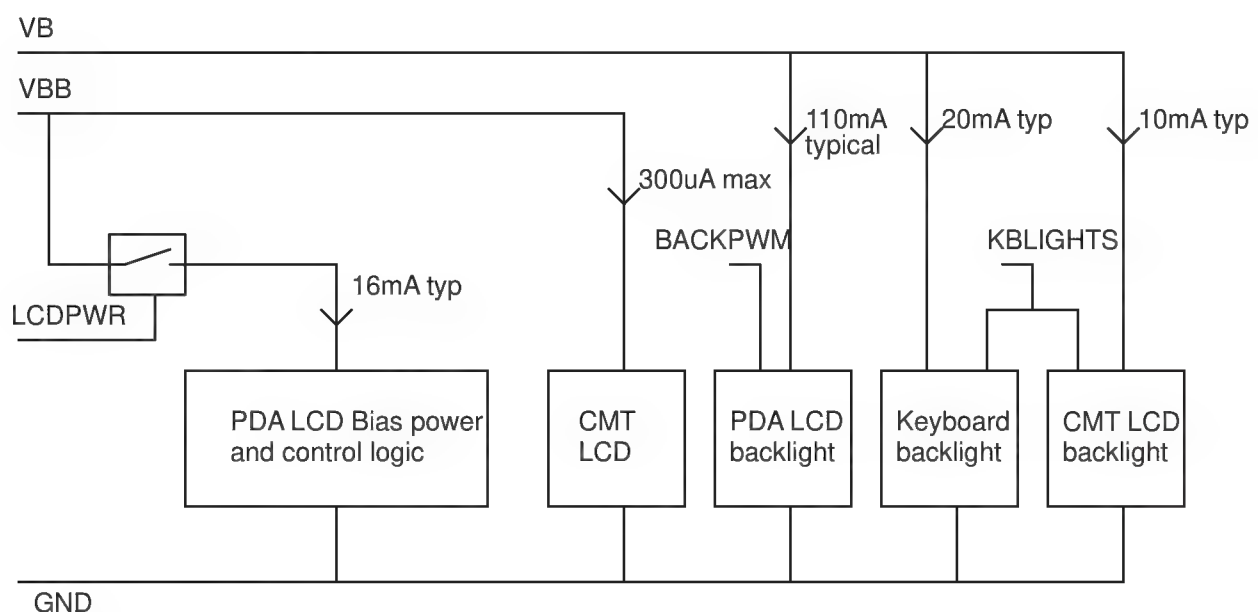


Figure 2. Power distribution and control signals of UL2.

DL2 Circuit Description

The module is connected via a 50 way FPC to the BL8 system logic.

The module includes following main blocks:

- CMT keyboard geometries.
- Switches for PDA soft keyboard
- Backlight LEDs for CMT keypad and CMT LCD illumination.
- CMT LCD.
- PDA LCD module.
- PDA LCD backlight circuit.
- PDA LCD power circuit.
- PDA LCD interface control logic.
- Hinge flex connector.
- Antenna connector and ground plane.

Keypad scanning.

There is 26 keys located in DL2 module. 6 PDA soft keys are located inside the lid and 20 CMT keys on the outer side. All these keys are in the same keyboard matrix as the QWERTY-keypad in the UL8 module.

Col(0–4) are used as column lines in keypad. Row(0–4 and 6) are used as row lines.

When a key is pressed the MCU gets an interrupt from a row and starts scanning. One column at a time is written low and rows are used to read which key is pressed.

CMT keypad and CMT LCD backlight

The CMT keypad and CMT display are illuminated with LEDs. Each LED is driven by a separate drive transistor.

LEDs for CMT display are driven with approximately 5mA each.

LEDs for CMT keymat illumination are driven with approximately 2.5mA each.

CMT LCD

Mechanical structure

LCD includes the frame, LCD cell with driver chip, reflector, adhesive tapes, and lightguide. The LCD is electrically connected to the UL2 PWB with a FPC and board-to-board connector.

The frame includes clips to mechanically attach the display to the UL2 PWB and also keep LCD cell and lightguide in place.

LCD cell specification

The LCD cell includes the display driver.

PDA LCD Module .

PDA LCD circuit main blocks are LCD glass including drivers, PDA LCD bias voltage power circuit and a control IC.

Parameter	Function
Display resolution	640 (x3) x 200 dots
Active area	107.52 x 33.6
Dot pitch	0.168 x 0.168mm
Display mode	D-TFD, Color, Transmissive
Frame frequency	51.5 Hz typical
Colors	4096 colors, 12-bit RGB
Display brightness	100nit (full brightness typical)

PDA LCD Backlight circuit

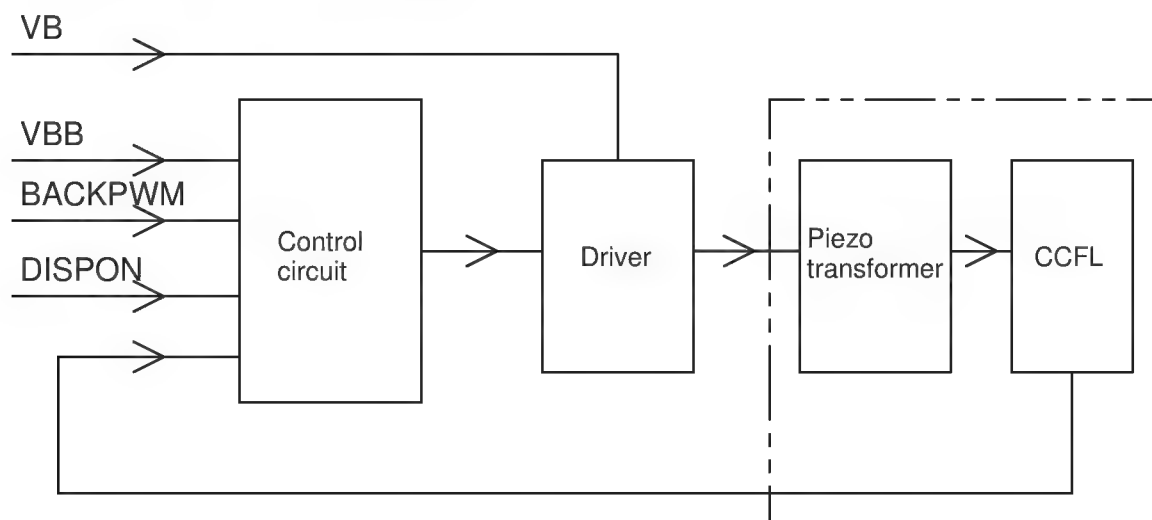


Figure 3. Backlight Power Supply

The **control circuit** generates a square wave input to the piezo driver circuit. This signal is maintained at the resonant frequency of the piezo transformer.

The **driver** is based around 2 FETs in Push–pull configuration. There is a single coil between the FETs and the piezo transformer.

Both FETs are turned off while the CCFL is off during dimming (BACKPWM low).

The **piezo transformer** part is soldered onto a FPC with the CCFL.

Piezo transformer characteristic	Value
Input voltage	8Vrms Max
Output power	1 W max
Output voltage	200 Vrms min
Output current	4.5mA
Operating current	1.5mA nominal
Operating frequency	130 +/- 10 kHz

The **CCFL lamp** is 2.6mm outer diameter and 1.8 mm inner diameter Double tube.

CCFL lamp characteristic	Value
Operating frequency	150 kHz (typ.)
Starting Voltage	About 500 Vrms
Operating Voltage	200 Vrms
Tube current	1 mA min , 3mA max
Operating current	1.5mA

PDA LCD Power circuit

PDA LCD power circuit generates the bias voltages necessary for the PDA display panel. Block diagram below.

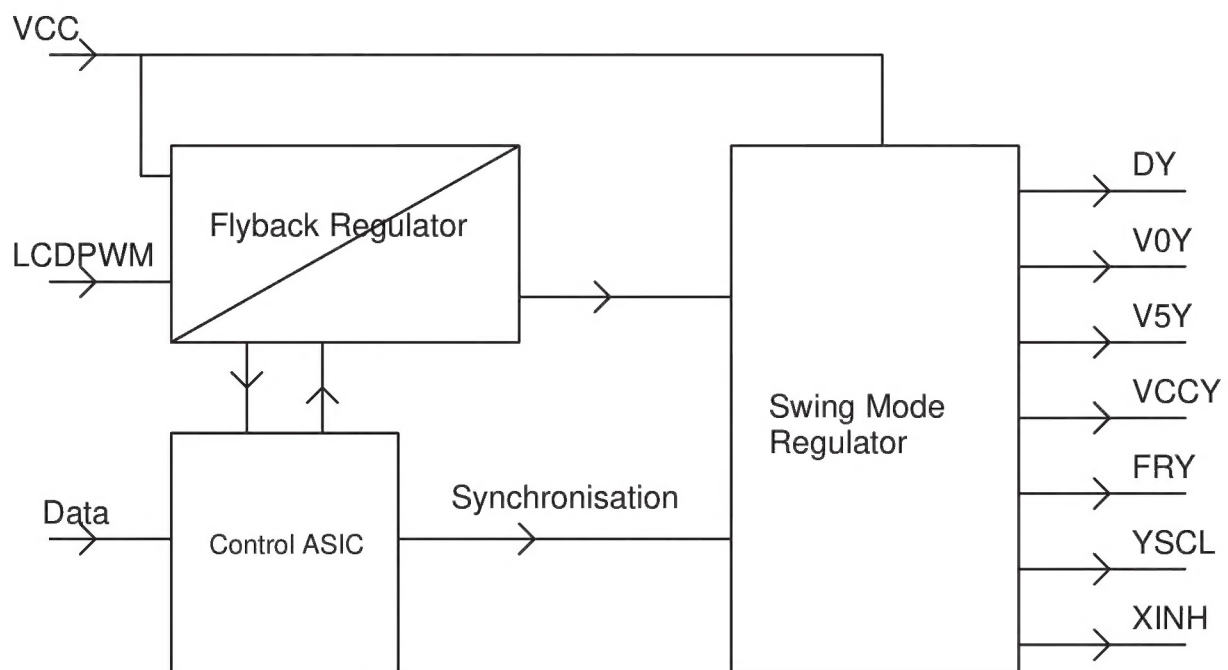


Figure 4. Block diagram of PDA Power Supply

The flyback regulator generates a negative bias voltage (Nominally -12V) from the battery voltage. The output of the flyback generator is temperature compensated and adjusted under software control.

The control ASIC handles the refresh of data to the PDA display panel and the generation of synchronisation signals for the swing mode regulator.

Antenna connectors and ground plane

The RF-signal from the external antenna connector/switch on BL8 is fed to the antenna via a coaxial cable that is led through the hinge. The signal is fed to the antenna through a coaxial connector and an antenna clip which are placed on the UL2 PWB.

The UL2 PWB includes the separate ground area that is required by the antenna.

QWERTY Keyboard Module UL8

General

UL8 is the combined QWERTY keypad/flex connection module. The base flex is single-sided, so all the components are on the same side of the flex.

Approximate component placement is shown below:

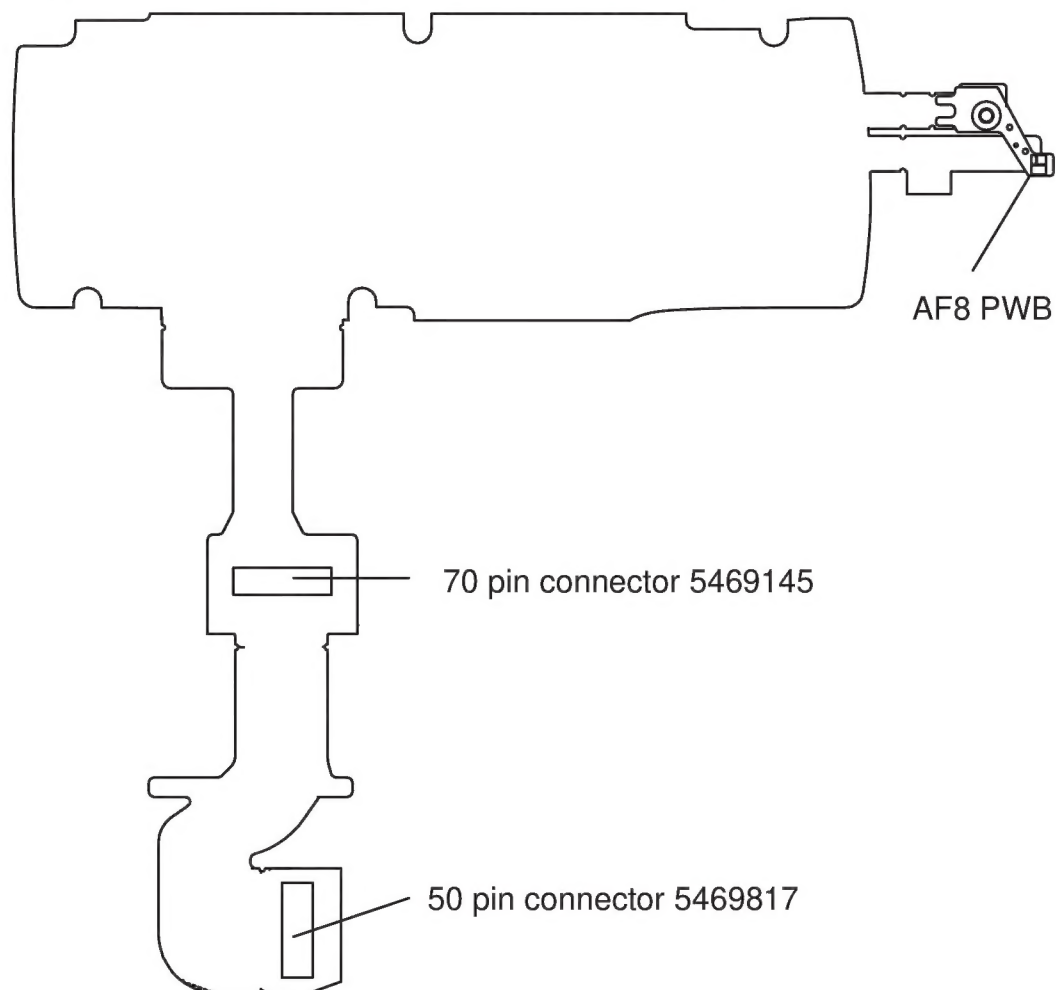


Figure 5. Component placement

AF8 PWB

AF8 is a small additional PWB to achieve "bull's eye" shaped pads for the ear-piece and connection for the battery removal switch. (Check that the RAE-3 software supports the battery removal switch feature.)

The approximate shape of AF8 is shown below.

One 22pF SMD capacitor is assembled to the AF8.

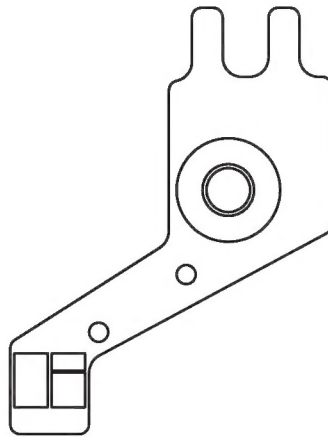


Figure 6. AF8 PWB